REMARKS

After entry of this amendment, claims 1-43 remain pending. In the present Office Action, claims 15-17, 26-28, 21, and 33 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-3, 6-7, 12-17, 21-28, 32-33, and 35 were rejected under 35 U.S.C. § 102(b) as being anticipated by Bonke et al., U.S. Patent No. 5,812,564 ("Bonke"). Claims 4-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bonke in view of Yoshimura, U.S. Patent No. 5,848,076 ("Yoshimura"). Claims 8, 18-20, and 29-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bonke. Claims 9-11 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bonke in view of Hetherington, U.S. Patent No. 4,995,041 ("Hetherington"). Applicants respectfully traverse these rejections and request reconsideration.

Art Rejections

Applicants respectfully submit that each of claims 1-43 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "execution circuitry configured to execute a first instruction which causes an access to first data in a memory; an error correction code (ECC) check circuit configured to detect an ECC error in response to the access to the first data in the memory; and ...the execution circuitry is further configured to execute the instructions in the microcode routine".

The Office Action alleges that Bonke teaches execution circuitry as the circuitry to the right of data bus 222 in Figure 5. This circuitry executes instructions supplied by the program ROM 202 and decoded by the instruction decode circuitry 214 and 215 (Bonke, col. 18, line 60-col. 21, line 23). However, the program ROM 202, decode circuitry 214 and 215, and execution circuitry to the right of data bus 222 are all part of the microcontroller 200 (see Bonke, Fig. 5 and col. 18, line 60-col. 21, line 23). The microcontroller 200 "is *dedicated* to *error computation and detection*" (Bonke, col. 18, lines 51-52). Accordingly, nothing in Bonke's microcontroller 200 teaches or suggests "execution circuitry configured to execute a first instruction which causes an access to first data in a memory [for which the ECC error is detected]". In Bonke, the accesses

which cause the ECC errors to be detected are generated from the host (see Bonke, description of Fig. 1).

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-22 depend from claim 1, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 2-22 recite additional combinations of features not taught or suggested in the cited art.

Claim 23 recites a combination of features including: "execution circuitry coupled to receive the instructions from the microcode unit, wherein the execution circuitry is configured to execute the instructions, and wherein the execution circuitry is also configured to execute a first instruction that causes an access to the first data in the memory, wherein the ECC error is detected during the access". The same teachings related to Bonke's microcontroller 200 discussed above are alleged to teach the above highlighted execution circuitry. Applicants respectfully submit that Bonke's execution circuitry in the microcontroller 200 fails to teach or suggest the above highlighted features of claim 23 as well.

For at least the above stated reasons, Applicants submit that claim 23 is patentable over the cited art. Claims 24-34 and 39-43 depend from claim 23, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 24-34 and 39-43 recite additional combinations of features not taught or suggested in the cited art.

Claim 35 recites a combination of features including: "performing an access to first data in a memory in response to executing a first instruction in execution circuitry; detecting an ECC error in response to the access; and dispatching a microcode routine stored by a microcode unit in response to the detecting, wherein the microcode routine includes instructions which, when executed in the execution circuitry, correct the ECC error in the memory". Applicants respectfully submit that Bonke's microcontroller 200 does not teach or suggest the above highlighted features either.

For at least the above stated reasons, Applicants submit that claim 35 is patentable over the cited art. Claims 36-38 depend from claim 35, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 36-38 recite additional combinations of features not taught or suggested in the cited art.

Section 112 Rejections

Claims 15 and 26 were rejected for including the phrase "the register the ECC error recorded in the register is valid". Applicants have amended claims 15 and 26 to recite "the ECC error is valid in the register". Applicants respectfully submit that the amendment overcomes the rejection. Claims 16-17 and 27-28 were rejected due to their dependence on claims 15 and 26, respectively, and thus the rejection is overcome for these claims as well.

Claim 21 was rejected for reciting the phrase "the ECC check circuit, if the access is a write which overwrites the ECC error in the memory, is configured to inhibit signaling the ECC error". The Office Action alleges that the phrase is "incompressible". Applicants respectfully submit that the original wording of claim 21 meets the requirements of 35 U.S.C. § 112. Nevertheless, Applicants have amended claim 21 to recite the equivalent: "the ECC check circuit is configured to inhibit signaling the ECC error if the access is a write which overwrites the ECC error in the memory". Applicants submit that the rejection of claim 21 is overcome.

Claim 33 was rejected for reciting the phrase "a reorder buffer coupled to receive a second indication indicating the ECC error, and wherein the reorder buffer is configured to generate the indication to the microcode unit responsive to retiring an instruction which generated, during execution, the access for which the ECC error is detected". The Office Action alleges that the phrase is "incompressible". Applicants respectfully submit that the original wording of claim 33 meets the requirements of 35 U.S.C. § 112. However, Applicants have amended claim 33 to be consistent with amendments to claim 23 (on which claim 33 depends). Claim 33 now recites "a reorder buffer coupled to receive a second indication indicating the ECC error, and wherein the

reorder buffer is configured to generate the indication to the microcode unit responsive to retiring the first instruction." Applicants respectfully submit that claim 33 as amended, meets the requirements of 35 U.S.C. § 112.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-75900/LJM. Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☒ Please debit the above deposit account in the amount of $144 for fees ($144 for 8 excess claims).

☐ Other:

Respectfully submitted,

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